REMARKS

Claims 1-35 were pending. Claims 1-4, 6-20, 22, 23, 26-33, and 35 have been amended for clarity. Claims 21 and 34 have been canceled. Claims 1-20, 22-33, and 35 are pending.

The Examiner's courtesy in conducting a personal interview with applicant's representative is acknowledged with appreciation. During the interview, the rejection based on Robertson et al. and the objection to the drawings were discussed. Applicant's representative explained the distinctions between the "pins" of Robertson et al. and the signal lines and shield lines of the present invention. The Examiner's interpretations of the claims and drawings were discussed. No agreement was reached.

An objection to the drawings under 37 C.F.R. § 1.83(a) is presented in the Office Action. As discussed during the interview, Applicant respectfully submits that every feature of the claims is shown in the drawings. The features of claim 1 are shown in FIG. 4, for example, as a "circuit element (58)," "a plurality of signal lines (BO, B1, B2, B3) supported by the circuit card (154)," and "a plurality of shield lines (60)." See specification paragraphs [00023] and [00024]. Withdrawal of the objection to the drawings is solicited.

Claims 1-2, 5-9, 11-12, 14-16, 18-21, 24, 26-27, 29-31, and 33-34 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Pat. No. 6,658,530 to Robertson et al. The rejection is traversed.

Claim 1 recites a circuit card including "a circuit element supported by the circuit card and having a plurality of inputs and outputs." The circuit card also includes "a plurality of signal lines supported by the circuit card," each "signal line being coupled respectively to one of said plurality of inputs or one of said plurality of

outputs." Also included is a "plurality of shield lines supported by the circuit card. The signal lines are "grouped in a plurality of adjacent corresponding pairs, a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines."

Robertson et al. discloses a circuit card (PCB 101) having a plurality of signal traces. The signal traces are connected to signal pins. Ground pins are located adjacent signal pins. The ground pins connect to a ground plane of PCB 101. See col. 3, lines 60-62. Robertson et al. postulates that the ground pins might improve signal integrity by reducing crosstalk between signal pins. Robertson et al. does not teach or suggest a circuit card having "a plurality of shield lines supported by the circuit card." Further, Robertson et al. also does not teach or suggest that the signal lines are "grouped in a plurality of adjacent corresponding pairs," with "a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines." Robertson et al. discloses only that ground *pins* may reduce crosstalk between signal line *pins*. Claim 1 is patentable over Robertson et al. Claims 2-5 depend from claim 1, and are patentable for at least the same reasons.

Claim 6 recites a circuit card featuring, *inter alia*, a "plurality of signal lines supported by the circuit card." Each signal line is "arranged and configured to be electrically and removably coupled at a first end respectively to one of a plurality of connectors of a connector device mounted on a printed circuit board." The circuit card also includes "a circuit element mounted on the circuit card and having a plurality of inputs and outputs." The signal lines are "coupled at a second end respectively to one of said plurality of inputs or outputs." Also included is a "plurality of shield lines supported by the circuit card," and "arranged and configured to be electrically and removably coupled at a first end to respective connectors of said connector device mounted on said printed circuit board." Each shield line is electrically coupled at a

second end to a respective one of either said plurality of circuit element inputs or outputs." The signal lines are "grouped in a plurality of adjacent corresponding pairs, a shield line being located respectively on each side of each of said plurality of corresponding pairs of said plurality of signal lines."

Robertson et al. does not disclose an arrangement of signal lines and shield lines such as that recited in claim 6 of the present application. The device disclosed by Robertson et al. features ground *pins* connected to a ground *plane*. Robertson et al. does not disclose a "plurality of shield lines supported by the circuit card, the shield lines being arranged and configured to be electrically and removably coupled at a first end to respective connectors of said connector device mounted on said printed circuit board, "and each shield line being" electrically coupled at a second end to a respective one of said plurality of circuit element inputs or outputs." Instead, according to Robertson et al., ground *pins* reduce crosstalk between signal *pins*. Claim 6 is patentable over Robertson et al. Claim 7 is dependent on claim 6, and is patentable for at least the same reasons.

Claim 8 recites a circuit card comprising, *inter alia*, "a plurality of signal lines having a length arranged and configured to connect between a connector and a circuit element, supported by the circuit card, to conduct signals therebetween, said plurality of signal lines being grouped in adjacent corresponding pairs." The circuit card also comprises "a shield line extending adjacent and the length of said plurality of signal line pairs to provide a shield, a shield line being located on each respective side of each corresponding pair of said signal lines."

Robertson et al. does not disclose the arrangement of shield lines and signal lines recited in claim 8 including "signal lines having a length arranged and configured to connect between a connector and a circuit element," "grouped in adjacent corresponding pairs," and "shield lines extending adjacent and the length of said

plurality of signal line pairs to provide a shield," "located on each respective side of each corresponding pair of signal lines." Claim 8 is patentable over Robertson et al. Claims 9 and 10 depend from claim 8, and are patentable for at least the same reasons.

Claim 11 recites a memory expansion card comprising "a memory device supported by the expansion card and having a plurality of inputs and outputs," and "a plurality of signal lines supported by the expansion card." Each of the "plurality of inputs and outputs of said memory device [is] coupled to a respective one of said signal lines." The signal lines are "grouped in a plurality of adjacent corresponding pairs." A plurality of shield lines is "electrically connected to said memory device, a shield line being located respectively between each pair of said plurality of corresponding pairs of said signal lines." The signal lines are "part of a bus system."

Robertson et al. discloses a card with ground pins connected to a ground plane. Robertson et al. does not teach "a shield line being located respectively between each pair of said plurality of corresponding pairs of said signal lines." Claim 11 is patentable over Robertson et al. Claims 12-14 depend from claim 11, and are patentable over Robertson et al. for at least the same reasons.

Claim 15 recites a memory expansion card comprising "a memory device supported by said expansion card and having a plurality of inputs and outputs," "a plurality of signal lines supported by said expansion card, each signal line connected respectively to one of said inputs or outputs, said plurality of signal lines being grouped in a plurality of adjacent corresponding pairs," and "a plurality of shield lines supported by said expansion card and electrically connected to said memory device, respective ones of said plurality of shield lines being located to extend along and between each of said plurality of corresponding pairs of said signal lines." The "plurality of signal lines is part of a bus system."

Robertson et al. does not disclose a memory expansion card which includes "a plurality of shield lines supported by said expansion card and electrically connected to said memory device, respective ones of said plurality of shield lines being located to extend along and between each of said plurality of corresponding pairs of said signal lines." Claim 15 is patentable over Robertson et al. Claims 16 and 17 depend from claim 15, and are patentable for at least the same reasons.

Claim 18 recites a memory expansion card assembly comprising "a connector device mounted on a motherboard and having a plurality of connectors, said plurality of connectors having a first portion for conducting signals and a second portion for providing a shield." The connectors in the first portion are "grouped in a plurality of corresponding pairs, a respective one of said connectors in said second portion being located between each of said plurality of corresponding pairs of said first portion of said plurality of connectors." A "plurality of signal lines on said expansion card" is "removably connected respectively to each of said first portion of connectors," "a plurality of shield lines on said expansion card being removably connected respectively to each of said connectors in said second portion and extending respectively along adjacent signal lines connected to said first portion of connectors." The first portion of connectors is "part of a bus system."

Robertson et al. does not disclose a memory expansion card assembly with "a connector device mounted on a motherboard and having a plurality of connectors, said plurality of connectors having a first portion for conducting signals and a second portion for providing a shield" which has "a plurality of shield lines" "being removably connected respectively to each of said connectors in said second portion and extending respectively along adjacent signal lines connected to said first portion of connectors." Claim 18 is patentable over Robertson et al.

Claim 19 recites a processing system having "a processing unit" and "a connector device having a plurality of connectors electrically connected to said processing unit." The circuit card includes "a circuit element supported by the circuit card and having a plurality of inputs and outputs." Each of a "plurality of signal lines supported by the circuit card" is "removably coupled respectively between one of said plurality of inputs and one of said plurality of connectors or one of said plurality of outputs and one of said plurality of connectors." A plurality of shield lines is "supported by the circuit card, each shield line being coupled respectively to said circuit element." The signal lines are "grouped in a plurality of adjacent corresponding pairs, a shield line being located between respective corresponding pairs of said signal lines." The "processing system comprises a bus system for passing signals through said processing system and said signal lines are coupled to said bus system."

Robertson et al. does not teach or suggest "a shield line being located between respective corresponding pairs of said signal lines." Claim 19 is patentable over Robertson et al. Claims 20 and 22-25 depend from claim 19, and are patentable for at least the same reasons as claim 19.

Claim 26 recites a processing system comprising, *inter alia,* a "processing unit," and "a memory expansion card coupled to said processing unit." The memory expansion card comprises "a memory device supported on said memory expansion card and having a plurality of inputs and outputs," "a connector device having a plurality of connectors for electrically coupling said memory expansion card to said processing unit," and "a plurality of signal lines and a plurality of shield lines supported by said memory expansion card for removable connection with said connector device." Each of "a first portion of said plurality of inputs and outputs of said memory device [is] coupled to a respective signal line to receive signals from or send signals to respective ones of said connectors of said connector device." The

"signal lines [are] grouped in a plurality of corresponding pairs," and a "shield line [is] located on each respective side of each of said plurality of corresponding pairs of said signal lines."

Robertson et al. does not teach or suggest a processing system that has "a shield line being located on each side of each of said plurality of corresponding pairs of said signal lines." Claim 26 is not anticipated by Robertson et al. Claims 27-29 depend from claim 26, and are patentable for at least the same reasons as claim 26.

Claim 30 recites a processing system having a memory expansion card as recited in claim 15, and is patentable over Robertson et al. for the same reasons. Claims 31 and 32 depend from claim 30, and are patentable for at least the same reasons as claim 30.

Claim 33 recites a method of constructing on a circuit card a bus system device comprising steps of "providing a circuit element on said circuit card, said circuit element having a first plurality of connectors for conducting bus signals," "grouping said first plurality of pins into a plurality of corresponding pairs," and "providing a second plurality of connectors on said circuit element." The second plurality of connectors is "connected to a respective shield line supported on said circuit card and extending along each side of respective pairs of signal lines supported on said circuit card and connected to each of said corresponding pairs of said first plurality of connectors."

Robertson et al. discloses a circuit card made by connecting ground pins to a ground plane. Robertson et al. does not teach manufacturing a circuit card by "providing a second plurality of connectors on said circuit element," the second plurality of connectors being "connected to a respective shield line supported on said circuit card and extending along each side of pairs of signal lines supported on said

circuit card and connected to each of said corresponding pairs of said first plurality of connectors." Claim 33 is patentable over Robertson et al. Claim 35 depends from claim 33 and is patentable for at least the same reasons.

Claims 3 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,216,205 to Chin et al. Applicant respectfully requests reconsideration of this rejection.

Claim 3 depends from claim 1, which is patentable over Robertson et al. Chin et al. has not been cited against claim 1. Even if Chin et al. had been properly cited against claim 1, the proposed combination of Robertson et al. and Chin et al. would not render the present invention obvious. Chin et al. has been cited as providing a driver to drive signals. Chin et al. is silent regarding the signal lines and shield lines of claim 1. Claim 1 and its dependent claims 2-10 are patentable over Robertson et al. in view of Chin et al.

Claim 22 depends from claim 19, which is patentable over Robertson et al. Chin et al. has not been cited against claim 19. Even if Chin et al. had been properly cited against claim 19, the proposed combination of Robertson et al. and Chin et al. would not render the invention of claim 19 obvious. Chin et al. has been cited as providing a driver to drive signals, and does not combine or motivate modification to provide signal lines that are "grouped in a plurality of adjacent corresponding pairs, a shield line being located between respective corresponding pairs of said signal lines." Claim 19 is patentable over the proposed combination of Robertson et al. and Chin et al. Claims 20 and 22-25 depend from claim 19, and are patentable for at least the same reasons.

Claims 4, 10, 13, 17, 23, 28, 32, and 35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,527,587 to Ortega et al. Applicant respectfully requests reconsideration of this rejection.

Claims 4 and 10 depend from claim 1, which is patentable over Robertson et al. Ortega et al. relates to differential signals, and has not been cited against claim 1. Ortega et al., even had it been properly cited against claim 1, does not combine with Robertson et al. to provide missing elements such as signal lines "grouped in a plurality of adjacent corresponding pairs," with "a shield line being located respectively on each side of each of said plurality of corresponding pairs of said signal lines." Claims 2-10 depend from claim 1, and are patentable for at least the same reasons.

Claims 13 and 17 depend from claim 11, which is patentable over Robertson et al. Ortega et al. has not been cited against claim 11. Ortega et al. teaches differential signals, and even had it been properly cited against claim 11, does not combine with or motivate modification of Robertson et al. to provide "a shield line being located respectively between each pair of said plurality of corresponding pairs of said signal lines." Claim 11, and its dependent claims 12-14, are patentable over the proposed combination of Robertson et al. and Ortega et al.

Claim 17 depends from claim 15, which is patentable over Robertson et al. Ortega et al. has not been cited against claim 15. Moreover, a *prima facie* obviousness rejection would not result from the combination. Ortega et al. has been cited as disclosing differential signals. Ortega et al. does not combine or motivate modification to provide "a plurality of shield lines being electrically connected to said memory device, a shield line being located respectively between each pair of said plurality of corresponding pairs of said signal lines." Claim 15, and its dependent claims 16 and 17, are patentable over Robertson et al.

Claim 23 depends form claim 19, which is patentable over Robertson et al. Ortega et al. has not been cited against claim 19. Ortega et al., even had it been properly cited against claim 19, does not combine with or motivate modification of Robertson et al. to provide signal lines that are "grouped in a plurality of adjacent corresponding pairs, a shield line being located between respective corresponding pairs of said signal lines." Claim 19, and its dependent claims 20 and 22-25, are patentable over the cited references to Robertson et al. and Ortega et al.

Claim 28 depends from claim 26, which is patentable over Robertson et al. Ortega et al. has not been cited against claim 26. Ortega et al., even had it been properly cited against claim 26, does not combine with or motivate modification of Robertson et al. to provide, for example, "a shield line being located on each respective side of each of said plurality of corresponding pairs of said signal lines." Claim 26 is patentable over the combination of Robertson et al. and Ortega et al. Claims 27-29 depend from claim 26, and are patentable for at least the same reasons.

Claim 32 depends from claim 30, which is patentable over Robertson et al. Ortega et al. has not been cited against claim 30. Ortega et al., even if it had been properly cited against claim 30, does not combine with or motivate modification of Robertson et al. to provide shield lines being "located to extend along each of said plurality of corresponding pairs of said plurality of signal lines." Claim 30 and its dependent claims 31 and 32 are patentable over the combined references to Robertson et al. and Ortega et al.

Claim 35 depends from claim 33, which is patentable over Robertson et al. Ortega et al. has not been cited against claim 33. Ortega et al., even had it been properly cited against claim 33, does not combine with or motivate modification of Robertson et al. to provide a method of making the second plurality of connectors "connected to a respective shield line supported on said circuit card and extending

along each side of respective pairs of signal lines supported on said circuit card and connected to each of said corresponding pairs of said first plurality of connectors." Claim 33 is patentable over Robertson et al. combined with Ortega et al. Claim 35 depends from claim 33, and is patentable over the cited references as well.

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of U.S. Pat. No. 6,526,462 to Elabd. Applicant respectfully requests reconsideration of this rejection.

Claim 25 depends from claim 19, which is patentable over Robertson et al. Elabd has not been cited against claim 19, and even if it had been properly cited, would not combine with or motivate modification of Robertson et al. to obtain the invention of claim 19. Elabd has been cited as implementing a processor, memory, and control circuit, for example, on a single chip. Elabd does not teach or suggest signal lines that are "grouped in a plurality of adjacent corresponding pairs, a shield line being located between respective corresponding pairs of said signal lines." Claim 19 and its dependent claims 20 and 22-25 are patentable over the proposed combination of Robertson et al. and Elabd.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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